

Application No.: 09/851,324

Docket No.: 21776-00057-US

REMARKS

Claims 22-26 remain pending in this Divisional Application. Claims 22 and 23 are independent. No claims have been amended, canceled, or added by this response.

IDS Reference & Request for Information Under 37 C.F.R. § 1.105

With respect to the Examiner's comments concerning the previously submitted IDS and the Examiner's Request for Information under 37 C.F.R. §1.105, an IDS has been submitted concurrently with this Response to provide a copy of the "NIKKEI MICRODEVICES" reference cited in the parent application ser. no. 09/350,125, now issued as U.S. Patent 6,509,645B2. A statement of relevance for this Japanese language reference has also been provided.

Entry and consideration of this reference by the Examiner is requested.

Unpatentability Rejections over Ishikawa, Kanatake, and Hotchkiss

Withdrawal of the rejection of claims 22 and 26 as being unpatentable over Ishikawa (US 5,955,776) in combination with Kanatake (US 6,178,654) and Hotchkiss (US 5,028,546) is requested. The applied art, either alone or in combination, does not teach or suggest all the claimed limitations.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.¹ Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.²

¹ See MPEP §2143.

² In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and See MPEP §2143.

Application No.: 09/851,324

Docket No.: 21776-00057-US

An essential evidentiary component of an obviousness rejection is a teaching or suggestion or motivation to combine the prior art references.³ Combining prior art references without evidence of a suggestion, teaching or motivation simply takes the inventors' disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight.⁴

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."⁵ Further with regard to the level of skill of practitioners in the art, there is nothing in the statutes or the case law which makes "that which is within the capabilities of one skilled in the art" synonymous with obviousness.⁶ The level of skill in the art cannot be relied upon to provide the suggestion to combine references.⁷

In one aspect of Applicants' disclosed and claimed invention, conductive balls for forming bumps are transferred by thermo-compression bonding to an electrode of a spherical semiconductor element using a temporary arrangement substrate which establishes a desired gap between a surface of the arrangement substrate and a surface of the spherical semiconductor element.

Turning now to the Ishikawa reference, and although nominally directed to spherical-shaped semiconductor integrated circuits, Ishikawa is directed to reducing or eliminating the restrictive manufacturing processes, expensive equipment, and stringent assembly and packaging requirements conventionally required for flat semiconductor chip manufacture.

As admitted in the Official Action, Ishikawa is silent as to a method to fabricate a spherical semiconductor device having spherical bumps on surface electrodes of a spherical semiconductor element in which an arrangement substrate sets a desired gap between the arrangement substrate and the semiconductor element, and in which the conductive balls are joined by thermo-compression bonding.

³ *C.R. Bard, Inc. v. M3 Systems, Inc.*, 48 USPQ2d 1225 (Fed. Cir. 1998)

⁴ *Interconnect Planning Corp. v. Feil*, 227 USPQ 543 (Fed. Cir. 1985)

⁵ See MPEP §2143.01, citing *In re Rouffet*, 149 F.3d, 1350, 1357, 47 USPQ2d 1453, 1457-8 (Fed. Cir. 1998).

Application No.: 09/851,324

Docket No.: 21776-00057-US

The Examiner offers Kanatake (FIG. 4, col. 3, lines 1-4) as teaching use of an arrangement substrate which sets the desired gap between the arrangement substrate and the semiconductor element. These two sections of the reference do not appear to be reasonably related, as discussed below.

Closer evaluation of this reference reveals that Kanatake is merely directed to a method and system for aligning spherical-shaped objects which uses "hollows" and "knobs" for alignment, while no mention at all is made of forming bumps.

In particular, Kanatake teaches a system and method for holding and aligning spherical shaped devices. The system aligns spherical shaped devices that have at least two hollows formed on an outer surface thereof. The system includes a first knob for aligning with the first hollow and a second knob for aligning with the second hollow. The first knob is relatively small, as compared with the first hollow, while the second knob is relatively large, as compared with the second hollow. The system may also include a third knob for securing the spherical shaped device with the first and second knobs..

As for the disclosure cited by the Examiner at col. 3, lines 1-4, Kanatake's Summary of the Invention section teaches that the system may include an ultrasonic vibrator capable of vibrating one or more of the three knobs, i.e., if a spherical shaped device is on the three knobs, the device would be levitated by the vibrations and moves to facilitate the alignment of the device to the knobs.

As for FIG. 4 of Kanatake, another embodiment is illustrated, as described at col. 5, lines 30-67. In this embodiment, sphere 10' includes three circularly shaped recesses or hollows 16', 18', and 20'. In FIG. 4, another embodiment of receptacle 24' is used with sphere 10', which includes knob pattern 36 formed, for example, from a single piece of material. Knob pattern 36 includes three "partial" pins 26', 28', and 30'.

⁶ *Ex parte Gerlach and Woerner*, 212 USPQ 471 (PTO Bd. App. 1980).

⁷ See MPEP §2143.01, citing *Al-Site Corp. v. VSI Int'l Inc.*, 50 USPQ2d 1161 (Fed. Cir. 1999).

Application No.: 09/851,324

Docket No.: 21776-00057-US

Sphere 10' is placed upon receptacle 24' for stabilizing the sphere and positioning it for further processing. Hollow 16' aligns with pin 26'; hollow 18' aligns with pin 28', and hollow 20' aligns with pin 30' to effect the alignment. There is no teaching or suggestion of conductive balls in Kanatake.

It is clear that Kanatake does not make up for the deficiencies of Ishikawa admitted by the Examiner, and it is also clear that Kanatake does not teach or suggest the claimed

"temporarily arranging conductive balls for forming said spherical bumps on an arrangement substrate at positions respectively corresponding to said surface electrodes; and transferring said conductive balls onto said surface electrodes to join the electrodes, wherein said conductive balls are transferred from said arrangement substrate to said surface electrodes while the position of each of said conductive balls on said arrangement substrate is controlled, wherein said conductive balls are transferred from said arrangement substrate to said surface electrodes such that a desired gap is formed between a surface of said arrangement substrate and a surface of said spherical semiconductor element...",

as recited in pending independent claim 22.

The Examiner also admits that Ishikawa and Kanatake are deficient with respect to teaching or suggesting the claimed "...wherein said conductive balls are transferred onto and joined to said surface electrodes by thermo-compression bonding."

Hotchkiss at col. 2, lines 35-39 is offered by the Examiner as teaching joining solder balls to electrodes by a thermo-compression process, and that it would have been obvious to use "well-known" thermo compression bonding process to bond the solder balls to the electrodes in order to provide an economical and efficient means of making contact with external devices.

Hotchkiss actually teaches affixing an aluminum foil pad to each of a plurality of Si spheres mounted in a foil matrix.

At the cited location in the reference (Summary of the Invention, col. 2, lines, 35-39), Hotchkiss is described as providing a method for affixing a foil pad to each of a plurality of silicon spheres mounted in a foil matrix. In the first step, a cell sandwich is formed comprised of

Application No.: 09/851,324

Docket No.: 21776-00057-US

an upper pad, the foil matrix with the mounted silicon spheres, a foil and a plate. In the next step, the cell sandwich is compressed to a first pressure. Next, the pressurized cell sandwich is heated to a predetermined temperature. In the next step, the heated cell sandwich is compressed to a second pressure greater than the first pressure for a period of time sufficient to fuse the foil to the silicon sphere. Finally, the excess foil is removed leaving a foil pad affixed to each of the silicon spheres.

Applicants submit that the above referenced citation proffered by the Examiner does not reasonably teach or suggest the claimed limitation of "...wherein said conductive balls are transferred onto and joined to said surface electrodes [of a spherical semiconductor element] by thermo-compression bonding", as recited in independent claim 22.

As the applied art does not teach or suggest all the limitations claimed in independent claim 22, withdrawal of the rejection and allowance of claim 22 are requested. Since dependent claim 26 depends from allowable claim 22, dependent claim 26 is submitted as being allowable at least on that basis, without further recourse to the additional patentable features recited therein.

Allowance of claims 22 and 26 is requested.

Unpatentability Rejections over Ishikawa, Kanatake, Hotchkiss and Yeh et al.

Withdrawal of the rejection of claims 23-25 as being unpatentable over Ishikawa (US 5,955,776) in combination with Kanatake (US 6,178,654), Hotchkiss (US 5,028,546), and Yeh et al. (US 5,803,340) is requested. The applied art, either alone or in combination, does not teach or suggest all the claimed limitations, and Yeh et al. is not properly combinable, as discussed below.

The various legal criteria for unpatentability rejections are stated above.

Applicants submit that the addition of Yeh et al. in the combination of references does not make up for the previously identified deficiencies of Ishikawa, Kanatake, and Hotchkiss. In particular, and although Yeh et al. may disclose use of composite solder paste to form solder joints in flip-chip integrated circuit devices, Yeh et al. does not teach or suggest a method for

Application No.: 09/851,324

Docket No.: 21776-00057-US

fabricating a spherical semiconductor device having spherical bumps on surface electrodes of a spherical semiconductor element, which includes, among other features, "...temporarily arranging conductive balls for forming said spherical bumps on an arrangement substrate at positions respectively corresponding to said surface electrodes [of a spherical semiconductor element]...", as recited in independent claim 23.

Applicants submit that Yeh et al. is not properly combinable with Ishikawa, Kanatake, and Hotchkiss, as Yeh et al. is directed to the solution of a completely different technical problem, i.e., flip-chip bumping, and not connection of spherical semiconductor devices.

Accordingly, reconsideration and allowance of claim 23 are requested. As dependent claims 24 and 25 depend from allowable claim 23, these claims are submitted as being allowable at least on that basis, without further recourse to the additional patentable features recited therein.

Conclusion

In view of the above, each of the presently pending claims 22-26 in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

For any fee that is due, please charge our Deposit Account No. 22-0185, under Order No. 21776-00057-US from which the undersigned is authorized to draw.

Respectfully submitted,

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